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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,484	01/27/2004	Atsuhiro Mori	61282-059	6279

7590 09/12/2006

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,484	MORI, ATSUHIRO	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-7 are pending in the Application.

Claims 1-7 are rejected.

Response to Amendment

2. Applicant's arguments, filed 19 July 2006, with respect to the rejection(s) of claim(s) 1-7 under 35 USC § 102(b) presented in the previous Examiner's Office action mailed on 19 April 2006 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejection are made, and presented below.

Specification

3. The abstract of the disclosure is objected to because it exceeds the maximum of 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 recites in part "access arranging means for causing the clock for the second data input/output means to wait" (lines 10-11 of this claim). This limitation renders the claim nonenabling, as one of ordinary skill in the art would not be able to ascertain how exactly a clock can "wait". More specifically, one of ordinary skill in the art would be unable to determine if the clock "wait" stage entails physically stopping the clock cycles, or preventing the ongoing cycles to propagate to the shared memory. Such a determination could not be rendered by one of ordinary skill in the art without undue experimentation pursuant to Applicant's description in the specification. Paragraph 0013 of Applicant's original specification describes causing the clock signal to wait, however it is unclear what exactly this waiting entails.

Claims 2 and 5-7 are rejected based on the same rationale as claim 1.

Claim 1 additionally recites in part "starting the access of the second data input/output means after the access of the first data input/output means is ended" (lines 15-16). This limitation renders the claim nonenabling, as one of ordinary skill in the art would not be able to ascertain how access of the second data input/output means can be started if the clock remains in a "wait" state per the previous limitation (regardless if said wait is physically stopping the clock, or preventing ongoing cycles to propagate to the memory as per Examiner's speculation, *supra*).

Claim 3 is rejected based on the same rationale as claim 1 (see line 8). More specifically, access to the processor is not possible while the clock is in a "wait" state, even after access of said input/output control means completes.

Claim 4 is rejected for inheriting the deficiencies claim 1.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites in part "access arranging means for causing the clock for the second data input/output means to wait" (lines 10-11 of this claim). This limitation renders the claim indefinite, as it would be unclear to one of ordinary skill in the art if the clock "wait" stage entails physically stopping the clock cycles, or preventing the ongoing cycles to propagate to the shared memory.

Claims 2 and 5-7 are rejected based on the same rationale as claim 1.

Claim 5 recites in part "executing the access of the first data input/output means earlier" (lines 9-10). This limitation renders the claim indefinite, as it would be unclear to one of ordinary skill in the art what the executing the access of the first data input/output means is executed earlier than. Examiner assumes Applicant intended the access of the first data input/output means to be executed earlier than the second data input/output means.

Claims 3- 4 are rejected for inheriting the deficiencies claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fadavi-Ardekani et al. (US Patent 6,499,087 B1), hereinafter Fadavi-Ardekani, and in further view of Tietjen (US Patent 4,780,843).

As for claim 1; Fadavi-Ardekani teaches an information processing apparatus comprising:

data storing means (Fig. 1, element 200);

first and second data input/output means for giving access to the data storing means (Fig. 1, elements 100 and 104);

clock generating means for supplying a clock from the second data input/output means (Fig. 1 depicts clock signals between the agents and the switch, and likewise between the switch and the memory);

switching means for switching access of the first data input/output means and the second data input/output means to the data storing means (Fig. 1, element 102); and

access arranging means for causing the clock for the second data input/output means to wait and executing the access of the first data input/output means earlier when a contention of the access of the first data input/output means and the second data input/output means to the data storing means is generated, and for starting the access of the second data input/output means after the access of the first data input/output means is ended (Fadavi-Ardekani teaches each agent as having it own unique clock. The clock of one agent must enter a wait state to allow the other agent to access the memory. The wait state is generated to avoid contention among the multiple agents. Once one agent completes access, the other agent can access the memory. col. 1, line 61 through col. 2, line 10).

Despite these teachings, Fadavi-Ardekani fails to specifically teach the clock generating means as supplying the clock *from* (emphasis added) the second data input/output means. Rather, Fadavi-Ardekani teaches the processor itself as generating the clock and sending it to the memory.

Tietjen however teaches a wait mode power reduction system and method for a data processor wherein a clock signal is generated and externally supplied to the processor to enable the processor to either continue operation, or wait (i.e. stop mode) – col. 1, lines 25-52. Additionally note Tietjen teaches shutting down (i.e. completely stopping) the clock signal, which is consistent with Fadavi-Ardekani's means of entering a wait state.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fadavi-Ardekani to further include Tietjen's wait mode power reduction system into his own system of synchronous memory sharing based on cycle stealing. By doing so, Fadavi-Ardekani would benefit by improving his system's power consumption while one of his agents is in a wait state as taught by Tietjen in col. 1, lines 25-52.

As for claim 2, Fadavi-Ardekani teaches an information processing apparatus comprising:

a built-in memory (Fig. 1, element 200);

a processor for processing data stored in the built-in memory (Fig. 1, element 100);

clock generating means for supplying a clock signal from the processor (Fig. 1 depicts clock signals between the agents and the switch, and likewise between the switch and the memory);

input/output control means for executing access to the built-in memory from an external control device (Fig. 1, element 104 – super agent is capable of executing access to the memory); and

access arranging means for causing the clock signal to wait and carrying out access of the input/output control means with a priority when a contention of access of the processor and the input/output control means to the built-in memory is generated (Fadavi-Ardekani teaches each agent as having it own unique clock. The clock of one agent must enter a wait state to allow the other

agent to access the memory. The wait state is generated to avoid contention among the multiple agents. Once one agent completes access, the other agent can access the memory - col. 1, line 61 through col. 2, line 10. Also note Fadavi-Ardekani teaches designating a super agent which has priority over the other agent(s) – col. 3, lines 27-67 – a wait request signal is inherit to Fadavi-Ardekani's system in order for it to properly enable the agent that does not win access to the memory to enter in the wait state).

Despite these teachings, Fadavi-Ardekani fails to specifically teach the clock generating means as supplying the clock *from* (emphasis added) the second data input/output means. Rather, Fadavi-Ardekani teaches the processor itself as generating the clock and sending it to the memory. Additionally, Fadavi-Ardekani fails to teach generating a wait request signal to cause the clock signal to wait. Tietjen however teaches a wait mode power reduction system and method for a data processor wherein a clock signal is generated and externally supplied to the processor to enable the processor to either continue operation, or wait (i.e. stop mode) – col. 1, lines 25-52. Tietjen additionally teaches generating a stop signal to indicate for the processor stop processing (col. 2, line 51 through col. 3, line 6). Additionally note Tietjen teaches shutting down (i.e. completely stopping) the clock signal, which is consistent with Fadavi-Ardekani's means of entering a wait state.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fadavi-Ardekani to further include Tietjen's wait mode power reduction system into his own system of synchronous memory sharing based on cycle stealing.

By doing so, Fadavi-Ardekani would benefit by improving his system's power consumption while one of his agents is in a wait state as taught by Tietjen in col. 1, lines 25-52.

As for claim 3, Fadavi-Ardekani teaches the information processing apparatus according to claim 2, further comprising

selecting means for switching the access of the processor and the input/output control means to the built-in memory (Fig. 1, element 102),

wherein the access arranging means outputs a control signal to the selecting means when a request for the access of the input/output control means to the built-in memory is generated during the access of the processor to the built-in memory (each agent is connected to the switch/arbiter via the ADC (address, data, and control) lines which is used to permitted access to the memory via one and only one agent – see Fig. 1. When a super agent requires access, it is able to obtain uncontested priority without requiring the arbiter to grant access – col. 1, lines 40-67. In other words, the super agent asserts control over the arbiter to grant access to the memory), and

the selecting means receiving the control signal switches the access of the processor to the access of the input/output control means to the built-in memory (the switch/arbiter (Fig. 1, element 102) is capable of arbitrating access between the two agents, and selectively permitting control to one based on priority).

As for claim 5, Fadavi-Ardekani teaches memory access arranging method of an information processing apparatus including data storing means and first and second

data input/output means for giving access to the data storing means, comprising the steps of:

causing a clock for the second data input/output means to wait when a contention of the access of the first data input/output means and the second data input/output means to the data storing means is generated (Fadavi-Ardekani teaches each agent as having it own unique clock. The clock of one agent must enter a wait state to allow the other agent to access the memory. The wait state is generated to avoid contention among the multiple agents. Once one agent completes access, the other agent can access the memory. col. 1, line 61 through col. 2, line 10);

executing the access of the first data input/output means earlier (the super agent can access the memory while the other agents must wait, or similarly if two non-super agents contend for access, one will be granted access while the other will be required to wait – col. 3, lines 57-67); and

canceling the clock wait of the second data input/output means after ending the access of the first data input/output means, and executing the access of the second data input/output means (once the first agent has completed access, the wait state is released and the other agent is permitted to access the memory – col. 4, lines 16-53) .

As for claim 6, Fadavi-Ardekani teaches a memory access arranging method of an information processing apparatus including a processor for carrying out a pipeline processing over an instruction, a memory provided in the processor, and input/output control means for executing access to the memory with a higher priority than the processor, comprising the steps of:

causing a clock supplied to the processor to wait when a contention of access of the processor and the input/output control means to the memory is generated (Fadavi-Ardekani teaches each agent as having it own unique clock. The clock of one agent must enter a wait state to allow the other agent to access the memory. The wait state is generated to avoid contention among the multiple agents. Once one agent completes access, the other agent can access the memory - col. 1, line 61 through col. 2, line 10. Also note Fadavi-Ardekani teaches designating a super agent which has priority over the other agent(s) – col. 3, lines 27-67 – a wait request signal is inherit to Fadavi-Ardekani's system in order for it to properly enable the agent that does not win access to the memory to enter in the wait state);

switching the access of the processor to the access of the input/output control means to the memory (arbiter - Fig. 1, element 102 control which agents can access the memory); and

canceling the clock wait of the processor after ending the access of the input/output control means to the memory, and executing the access of the processor to the memory (once the first agent has completed access, the wait state is released and the other agent is permitted to access the memory – col. 4, lines 16-53).

Despite these teachings, Fadavi-Ardekani fails to teach generating a wait request signal to cause the clock signal to wait.

Tietjen however teaches a wait mode power reduction system and method for a data processor wherein a clock signal is generated and externally supplied to the processor to enable the processor to either continue operation, or wait (i.e. stop mode)

– col. 1, lines 25-52. Tietjen further teaches generating a stop signal to indicate for the processor stop processing (col. 2, line 51 through col. 3, line 6).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fadavi-Ardekani to further include Tietjen's wait mode power reduction system into his own system of synchronous memory sharing based on cycle stealing. By doing so, Fadavi-Ardekani would benefit by improving his system's power consumption while one of his agents is in a wait state as taught by Tietjen in col. 1, lines 25-52.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fadavi-Ardekani (US Patent 6,499,087 B1), in further view of Peters et al. (US Patent 6,065,102), hereinafter Peters.

As for claim 7, Fadavi-Ardekani teaches a memory access arranging method of an information processing apparatus having a processor for carrying out a pipeline processing over an instruction, a memory provided in the processor, input/output control means for executing access to the memory with a higher priority than the processor, and holding means for holding read data output from the memory before a wait operation of the processor during the wait operation of the processor, comprising the steps of:

causing a clock supplied to the processor to wait (Fadavi-Ardekani teaches each agent as having it own unique clock. The clock of one agent must enter a wait state to allow the other agent to access the memory. The wait state is generated to avoid contention among the multiple agents. Once one agent

completes access, the other agent can access the memory. col. 1, line 61 through col. 2, line 10);

executing the access of the input/output control means to the memory (the winning agent can access the memory once the arbiter grants access to the memory – col. 3, lines 26-67); and

canceling the clock wait of the processor after ending the access of the input/output control means to the memory, and restarting the access of the processor to the memory (once the first agent has completed access, the wait state is released and the other agent is permitted to access the memory – col. 4, lines 16-53).

Despite these teachings, Fadavi-Ardekani fails to teach holding the read data output from the memory in a holding means before the wait operation of the processor when a contention of read access of the input/output control means is generated. Additionally Fadavi-Ardekani fails to teach, supplying the data held in the holding means to the processor.

Peters however teaches a fault tolerant multiple client memory arbitration system which allows multiple clients to access data redundantly stored in two cache memories (col. 2, lines 53-65). In other words both the local cache memory and the redundant cache memory store the same data. The system further allows for the arbitration of access to either the local cache memory, or the mirrored cache memory. In other words, data can be extracted from alternative holding means (i.e. the mirrored cache) rather than the local cache itself depending on the status of the arbitration logic.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fadavi-Ardekani to further include Peters multiple client arbitration system into his own system of synchronous memory sharing based on cycle stealing. By doing so, Fadavi-Ardekani would be able to improve the fault tolerance of his memory system by proving redundant storage as taught by Peters in col. 1, lines 23-45.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Fadavi-Ardekani (US Patent 6,499,087 B1) and Tietjen (US Patent 4,780,843) as applied to claim 3 above, and in further view of Peters (US Patent 6,065,102).

As for claim 4, though the combined disclosure of Fadavi-Ardekani and Tietjen meet all the limitations of claim 2, they fail to specifically teach, holding means for holding read data output from the built-in memory before a wait operation of the processor during the wait operation of the processor, wherein the access arranging means switches read data to be supplied to the processor between the read data output from the built-in memory and the read data held by the holding means as recited in this claim.

Peters however teaches a fault tolerant multiple client memory arbitration system, which allows multiple clients to access data redundantly stored in two cache memories (col. 2, lines 53-65). In other words both the local cache memory and the redundant cache memory store the same data. The system further allows for the arbitration of access to either the local cache memory, or the mirrored cache memory.

In other words, data can be extracted from alternative holding means (i.e. the mirrored cache) rather than the local cache itself depending on the status of the arbitration logic.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fadavi-Ardekani to further include Peters multiple client arbitration system into his own system of synchronous memory sharing based on cycle stealing. By doing so, Fadavi-Ardekani would be able to improve the fault tolerance of his memory system by proving redundant storage as taught by Peters in col. 1, lines 23-45.

Response to Arguments

9. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new grounds of rejection presented *supra*.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER